What is claimed is:

1. A computer system comprising:

a local bus;

a memory bus capable of indicating data; and

a buffer adapted to capture the data directly from the memory bus, the buffer being located closer to the local bus than to the memory bus.

2. The computer system of claim 1, wherein

the memory bus is capable of indicating a data strobe signal, and

the buffer is adapted to latch the data from the memory bus in response to the data strobe signal.

3. ~~The computer system of claim 1, further comprising:~~

conductive traces adapted to communicate indications of the data from a first region near the memory bus to a second region near the buffer, the conductive lines introducing an ~~approximate first asynchronous propagation delay in the communication~~.

4. The computer system of claim 3, further comprising:

circuitry adapted to transfer the data from the buffer to the local bus without introducing a second propagation asynchronous propagation delay that is greater than the first asynchronous propagation delay.

5. The computer system of claim 1, wherein the buffer is part of a local bus interface.

6. The computer system of claim 1, further comprising:

circuitry adapted to transfer the data from the buffer to the local bus, at least a portion of the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

7. The computer system of claim 1, wherein the buffer is part of a local bus interface that is coupled to the local bus, the computer system further comprising:

a third bus;

a fourth bus;

a third bus interface coupled to communicate with the third bus;

a fourth bus interface coupled to communicate with the fourth bus; and

a multiplexing circuit adapted to selectively cause the buffer to store other data from the third and fourth bus interfaces.

8. The computer system of claim 1, wherein the buffer is part of a local bus interface that is located closer to the local bus than to the memory bus.

9. The computer system of claim 8, wherein the local bus interface further comprises:

a local bus controller adapted to use the buffer to furnish signals to the local bus that indicate the data.

10. The computer system of claim 1, further comprising:

a memory interface located closer to the memory bus than to the local bus, the memory interface including another buffer to store other data to be furnished to the memory bus.

11. A bridge for use with a local bus and a memory bus capable of indicating data, comprising:

conductive traces adapted to communicate indications of the data from a first region near the memory bus to a second region near the local bus; and

a local bus interface being located closer to the local bus than to the memory bus, the local bus interface including a buffer adapted to capture the indications of the data from the conductive traces near the second region to directly capture the data from the memory bus.

12. The bridge of claim 11, wherein

the memory bus is capable of indicating a data strobe signal, and

the buffer is adapted to latch the data in response to the data strobe signal.

13. The bridge of claim 11, wherein the conductive traces introduce a first asynchronous propagation delay to the indications of the data, the bridge further comprising:

circuitry adapted to transfer the data from the buffer to the local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

14. The bridge of claim 13, further comprising:

circuitry adapted to transfer the data from the buffer to the local bus, at least a portion of the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

15. The bridge of claim 12, further comprising:

a third bus;

a fourth bus;

a third bus interface coupled to communicate with the third bus;

a fourth bus interface coupled to communicate with the fourth bus; and

a multiplexing circuit adapted to selectively cause the buffer to store other data from the third and fourth bus interfaces.

16. The bridge of claim 12, wherein the local bus interface further comprises:

a local bus controller adapted to use the buffer to furnish signals to the local bus that indicate the data.

17. The bridge of claim 12, further comprising:

a memory interface located spatially closer to the memory bus than to the local bus, the memory interface including another buffer to store other data to be furnished to the memory bus.

18. A method usable with a computer system that includes a local bus and a memory bus, the method comprising:

furnishing data to the memory bus in a memory read operation; and

capturing the data directly from the memory bus in a buffer that is located closer to the local bus than to the memory bus.

19. The method of claim 18, wherein the act of capturing comprises:

latching the data from the memory bus in response to a data strobe signal of the memory bus.

20. The method of claim 18, further comprising:

using conductive traces adapted to communicate indications of the data from a first region near the memory bus to a second region near the buffer, the conductive lines introducing an approximate first asynchronous propagation delay in the communication.

21. The method of claim 20, further comprising:

transferring the data from the buffer to the local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

22. A method usable with a computer system, comprising:

substantially extending a memory bus into a bridge, the memory bus being adapted to indicate data in a memory read operation; and

capturing the data directly from the extension of the memory bus into the bridge.

23. The method of claim 22, wherein the act of capturing comprises:

latching the data from the extension of the memory bus in response to a data strobe signal of the memory bus.

24. The method of claim 22, further comprising:

using conductive traces adapted to communicate indications of the data from a first region near the memory bus to a second region near the buffer, the conductive lines introducing an approximate first asynchronous propagation delay in the communication.

25. The method of claim 24, further comprising:

transferring the data from the buffer to a local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

26. The method of claim 22, wherein the act of extending comprises:

extending the memory bus into the bridge so that the extended end of the memory bus is closer to a local bus than to the portion of the memory bus that is located outside of the bridge.